# VIDEO LINE SELECTOR

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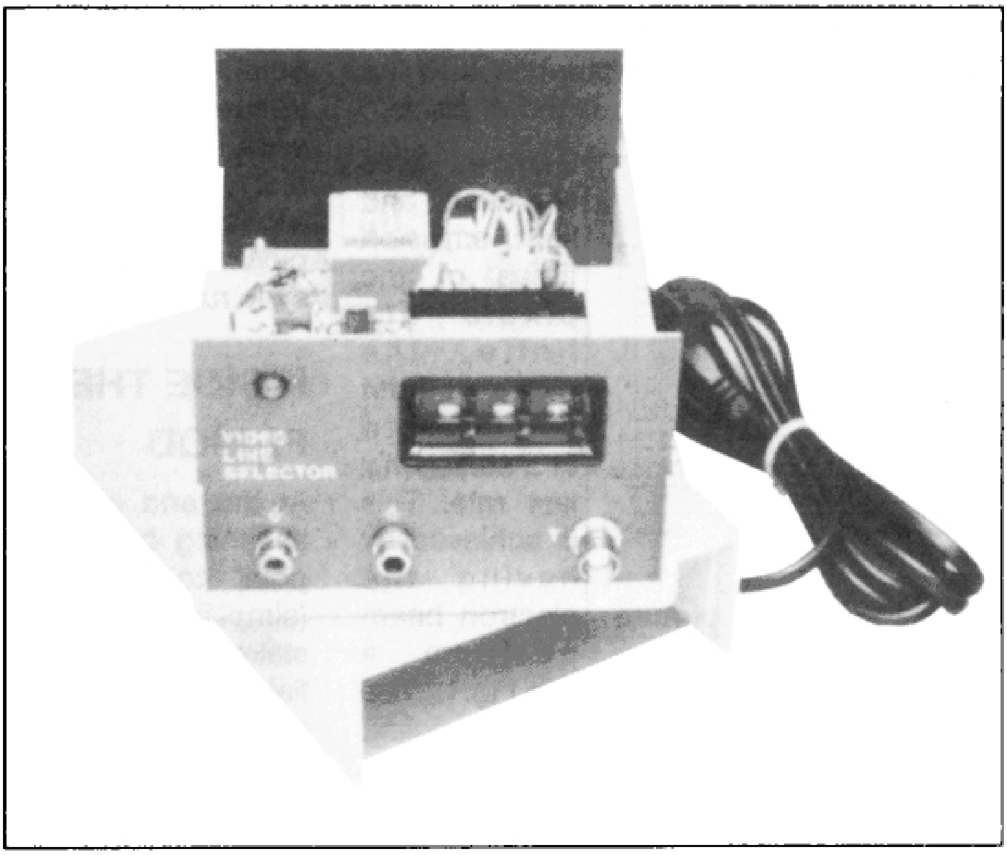
This low-cost line selector is a must for any one working on television and video circuits. The reason is plain: an oscilloscope, even when set to TV field or line triggering, will not usually allow you to study the video content of one specific line in the picture. This is simply because it is re-triggered by every next sync pulse instead of a single user-defined one.

The instrument described here ends the hassle by keeping your oscilloscope triggered on a video signal. Applications are manifold and interesting as you will soon discover. In particular, the "invisible" test lines transmitted as an extra service by most TV stations are indispensable for aligning video circuits as well as for bandwidth and picture quality assessment.

Although many oscilloscopes offer two timebase settings and associated sync separators for TV signals, these functions are often difficult to master for the beginner. For simple TV signals like a monochrome staircase, the TV field and line trigger modes are usually sufficient to ensure a reasonably stable oscilloscope display. For moving pictures, however, triggering is a constant nuisance. Furthermore, the oscilloscope user often has no idea which picture line he is monitoring.

The function of a video line selector is not unlike that of a word comparator for, say, a logic analyser. Both circuits allow the user to define a certain trigger condition for the displaying instrument (usually an oscilloscope). This condition is necessary to extract only the wanted information from a composite signal, and to prevent all other information arriving at the display, where it causes confusion and display irregularity. In the case of the logic analyser, the trigger condition is defined as a combination of logic levels.

In the case of the video line selector, it is



defined as the number of a specific line in the TV picture. The present circuit has a block of thumbwheel or other switches with BCD (Binary Coded Decimal) outputs to set up a trigger condition for any one of 625 lines (PAL - Phase Alternation Line) in an interlaced picture. As a result, the selected line is the first one displayed on the oscilloscope (depending on the timebase setting, more lines may follow).

## THE TV PICTURE

Although it is assumed here that the reader is familiar with the basic structure of a TV signal. a few essential points will be covered briefly in the interest of the circuit description. The discussion applies mostly to the PAL I/B/G TV standards.

A moving TV picture is not a series of still images projected on the screen in rapid succession. Rather, it is produced by the light emission of individual pixels (picture elements) at the inside of the picture tube. These pixels are actuated by a fast scanning electron beam. The intensity of this beam is accurately controlled to actuate certain pixels, while "skipping" adjacent ones. In this way the picture is built up from many hundreds of thousand of pixels.

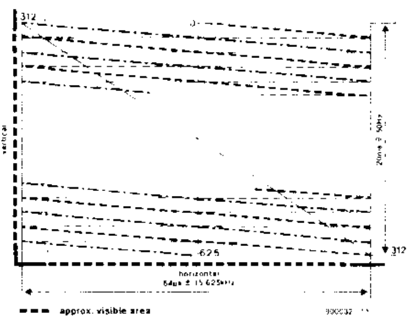


Fig.1 One TV picture

Since the actuation and light emission times of the pixels are finite, the picture must be refreshed at a sufficiently fast rate. This is achieved by having the electron beam perform a scanning movement as shown in Fig.1. The picture is, in fact, composed of two fields, which together form a raster or picture. To allow sufficient time for the blanked beam to travel from the bottom of a raster to the top of the next one, and to prevent display flicker, the scanning is interlaced, i.e. two fields are written in succession. After the blanking period (vertical flyback) the beam starts to write, in a zig-zag manner, the first (or "odd") field, starting at the top centre of the picture. The number of complete pictures (rasters) is 25 per second, which is obtained by displaying 50 interlaced fields per second.

Since a PAL picture consists of 625 lines, each field must have 312.5 lines to maintain the correct relationship with the other field due to interlacing. The sequence is, therefore, 1-314-2-315-3-316, etc. (Fig.1).

A number of lines at the top and bottom of the picture shown in Fig.1 fall inside the field blanking and are therefore not normally visible on the TV. On many older TV sets they can be made visible however, by reducing the picture height. In practice about 10% of the available number of picture lines (625 for PAL) fall within the vertical flyback (blanking) period, which contains the vertical synchronisation pulse and a number of other signals.

TV lines in a PAL picture have a duration of 64us, which corresponds to a line frequency of 15,625Hz. About 52us of each line contains picture information - the rest (invisible to the left and right) is allocated to the line blanking interval. One picture is built up in 20ms, i.e. the vertical sync runs at 50Hz.

## INSIDE THE FIELD BLANKING PERIOD

At the end of each field (312.5 lines) the scanning beam has to be repositioned to point to the top of the screen. The (simplified) drawings in Fig.2 show a staircase video signal in two successive fields. the raster synchronisation pulse starts at instant FDW (Field Datum Word), the datum word, and lasts 2.5H (H = one line period). A problem may occur with the line synchronisation which must continue

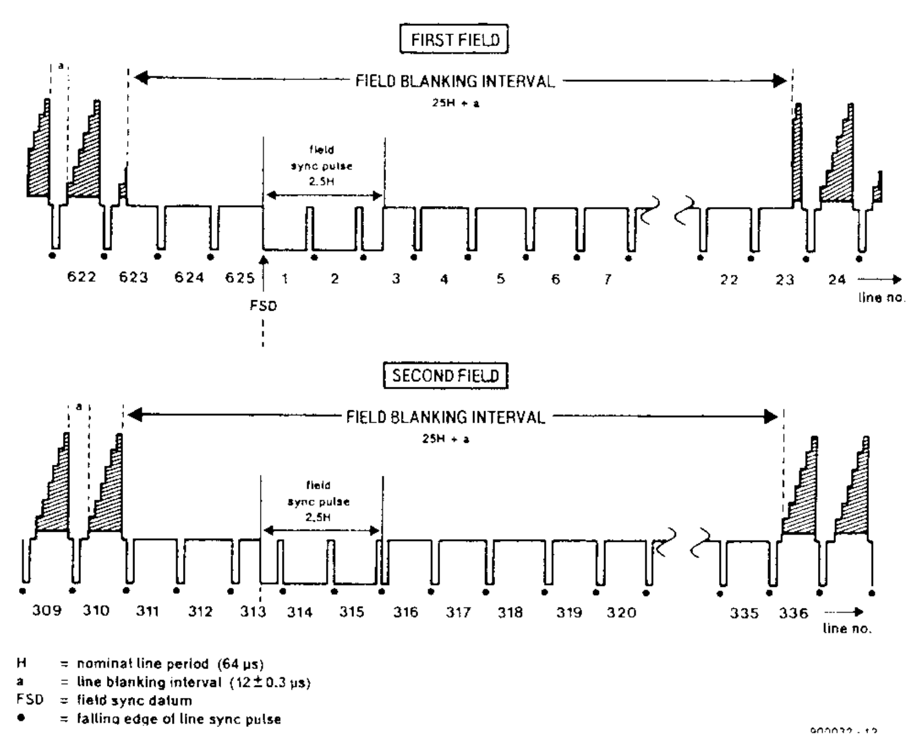


Fig.2 TV Field transistion without Equalising Pulses

during the filed synchronisation. Normally, in a composite video signal, the line synchronisation is detected as a pulse that goes lower than the reference black (or blanking) level. Since the field sync pulse already reaches the lowest possible level, the TV would miss out on a least 2 line sync pulses if they were not inserted "upside down" in the field sync interval. This can be done with impunity since most line sync processors in TV sets and monitors use the negative edge of the pulse (in Fig.2 these are marked with a small dot).

Since each raster consists of an odd number of lines, a field consists of an even number of lines plus one half line. This means that instant FDW coincides with the start of a full line (number 1) in the first field, and with the centre of a line (number 313) in the second field.

As a result, the inverted line sync pulses occur at different instants in the odd and even fields. Without special measures, this may lead to incomplete interlacing and, as a result, a light display flicker.

The cause of this (possible) problem lies with the synchronisation separator circuits in the TV. In general, the line and field sync signals are obtained in two ways with the aid of different circuits. The line sync is obtained by differentiating the sync pulse train, whereas the field sync is obtained by integrating the sync pulse train. Without going into details of these operations, it will be clear that the instant the field sync pulse for the first field arrives, it will be one line period (H) after the last line sync pulse. For the second field, however, it follows at only 32us (0.5H) after the last line sync pulse.

This situation would lead to timing problems with the regeneration of the field sync pulses (obtained from integration, which is a time-based operation) for the two fields, and, as a result, small, but visible, interlace imperfections.

The solution to this problem has been found in the use of equalising pulses, which precede and follow the field sync pulse as shown in Fig.3. These pulses, which are 2.53us long, are inserted into 2.5H long slots before and after the field sync pulse. The frequency of the equalising is 2 times that of the line frequency, while their width is half that of a line sync pulse.

The beneficial effect of the equalising pulses is that the integrator output voltages provided by the picture sync separator are made equal for both fields. The result is near-perfect interlaced scanning.

Although the first 20 lines after the field sync fall within the field blanking period, they are not normally empty (i.e. black with no video content). Indeed, the lines in the blanking period are often the most interesting to the video technician. Depending on the TV station and operating authorities, lines 15-21 and 328-334 usually contain special test signals. These video insertion (VIT - Video Insertion Test) signals may be fed to an oscilloscope to assess the reception quality or the response of certain sub-circuits in the receiver. In a number of cases, these lines are also used for remote monitoring of transmitter linearity and for information exchange between a central microwave distribution tower and TV relay stations. The use of these lines appears to be little-known, which makes them even more interesting (also for certain satellite transmissions).

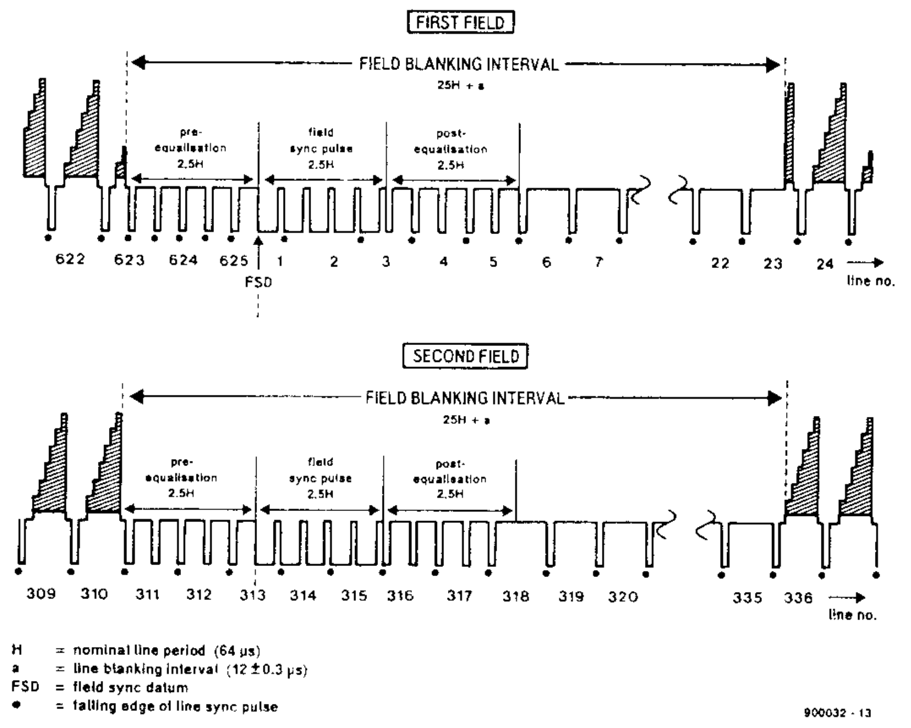


Fig.3 TV Field transistion with Equalising Pulses

In Europe, teletext is normally carried in lines 15, 16, 20, 21, 328, 329, 333 and 334.

## THE LINE SELECTOR CIRCUIT

The practical circuit on the video line selector is fairly simple -see Fig.4. The circuit may be divided into two parts: a sync separator (IC1 and IC2) and a counter plus word comparator (IC3-IC8).

The circuit has two inputs and one output. One of the inputs is for the composite video signal (CVBS - Chroma Video Blanking Synchronisation - at connector K1), and the other for the BCD switchblock (or discrete switches) used for setting the video line number.

The output supplies a CMOS-compatible digital signal with a swing of 5V for connecting to the trigger input of an oscilloscope.

The key component in the sync separator is IC1, a type LM1881 from National Semiconductors. This chip contains everything that is necessary to extract the synchronisation pulses from a composite video signal applied to its input, at pin-2. In addition, this chip is capable of identifying, on the basis of their different sync pulse structures, the odd and even fields that make up a raster. Only the BURST and ODD/EVEN outputs are used in the present application.

The BURST output goes low for about 4us to mark the approximate location of the chrominance colour burst (4.43 MHz for PAL; 3.58MHz for NTSC) on the back porch of the line blanking period. The burst pulse is used here for line counting, since the LM1881 lacks a line sync output. Provided the timing is corrected this can be done with impunity since every line blanking period has a rear porch (whether a burst is actually present in the CVBS signal is irrelevant here).

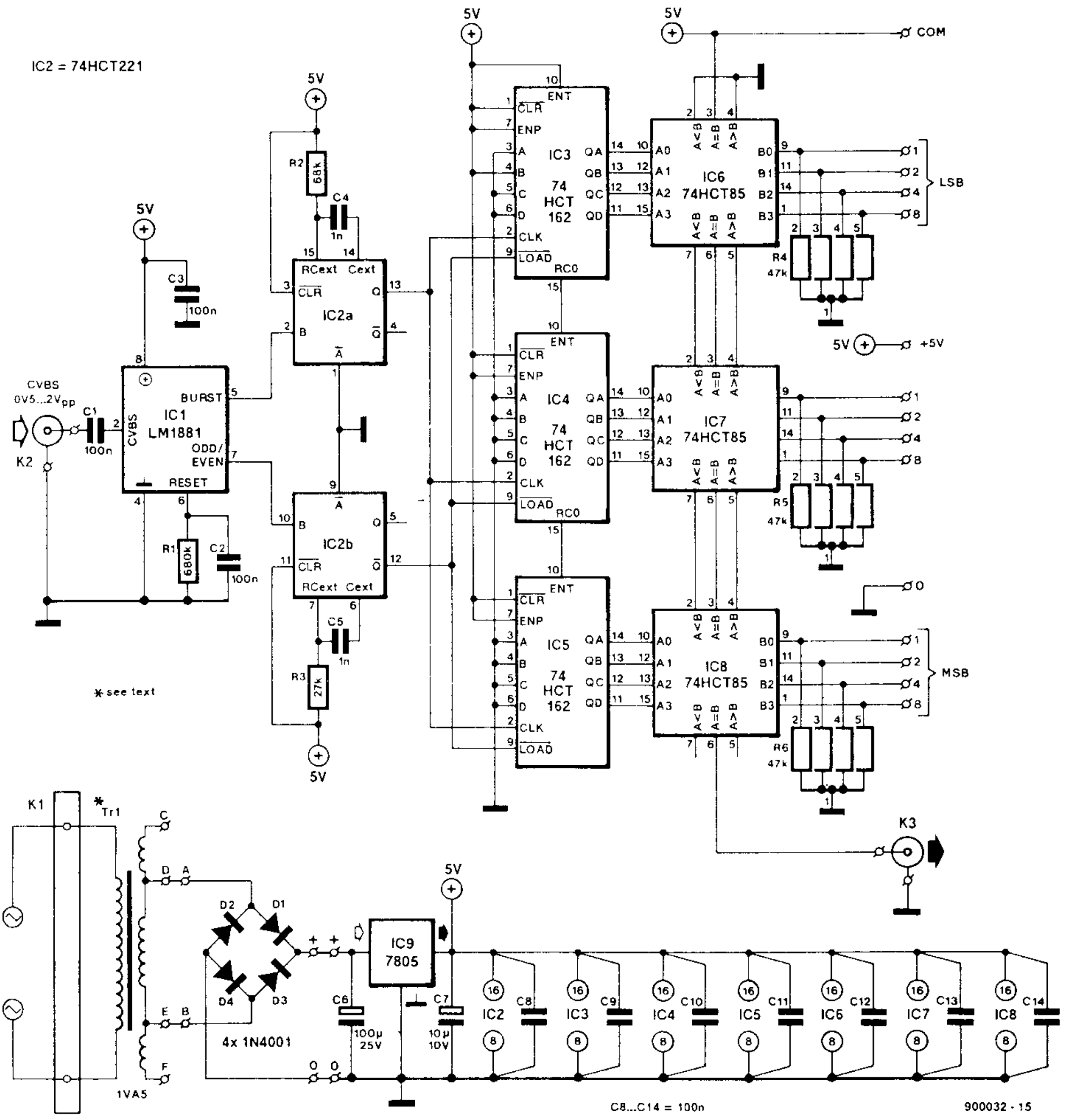


Fig.4 Circuit Diagram of the Video Line Selector

Both the ODD/EVEN and the BURST signals are lengthened by a non-retriggerable monostable contained in IC1.

The ODD/EVEN output toggles on the rising edge of the first equalising pulse in the field sync pulse for the first field. The counters in the word comparator, however, are preset on the falling edge of this pulse. Since that instance occurs half-way through the first line, a preset value of 2 (0010) is loaded into IC3 by tying its B-input to the +5V line.

The result, however, would be that triggering occurs half a line too early for the first 5 lines, which requires a correction at

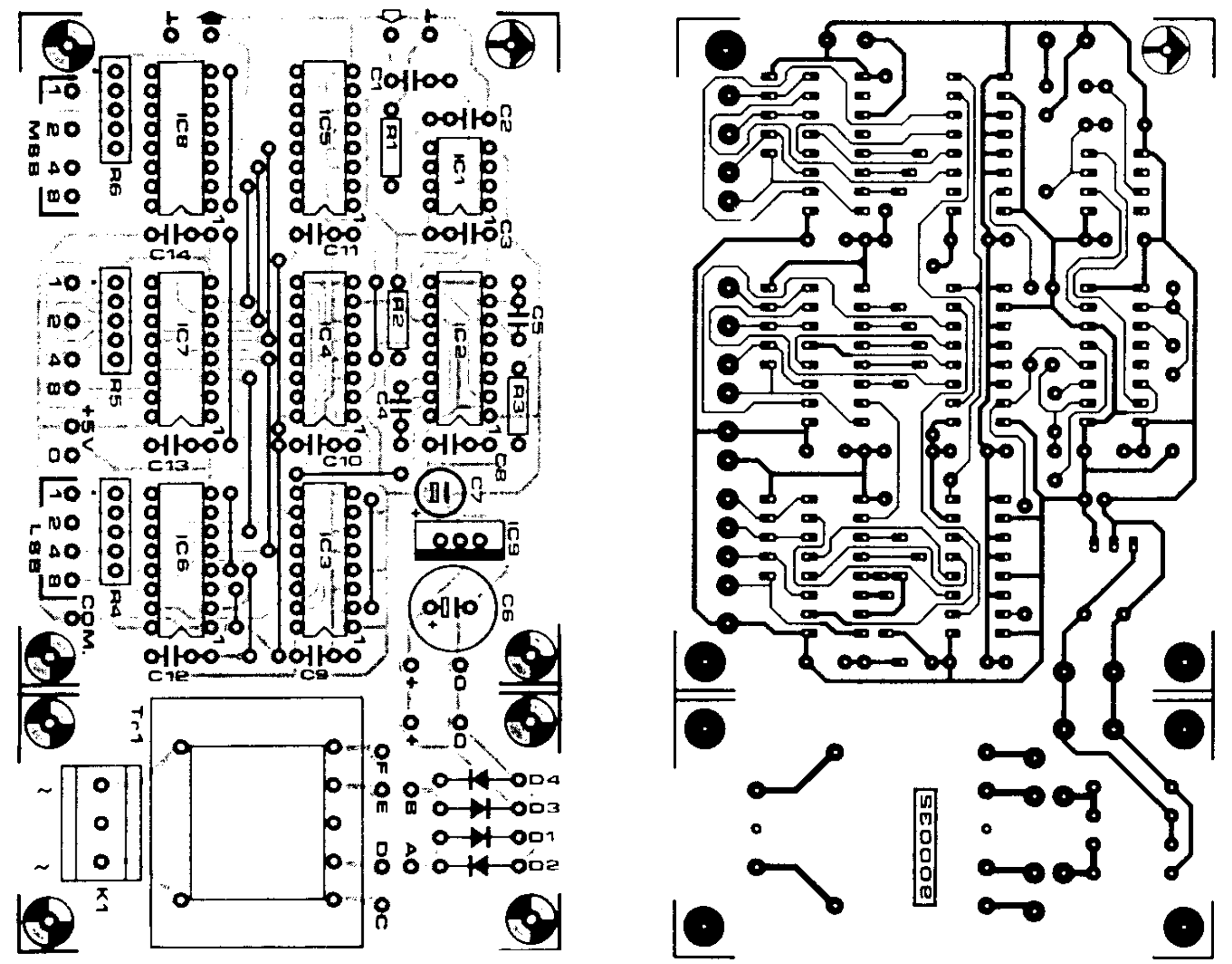


Fig.5 PCB layout

the end of the last equalising pulse. Timer IC2B is triggered on the rising edge of the ODD/EVEN signal. The bar-Q output of this timer is connected to the LOAD inputs of counters IC3, IC4 and IC5. These are actuated on the rising edge of the clock signal, when the preset values are loaded.

The BURST/BACK PORCH signal supplied by the LM1881 is not used direct for controlling the load operations in the counters. Instead, a non-retriggerable monostable, IC2A, is used to prevent the counters being advanced five lines too many by the equalising pulses. The monotime of IC2A is set to about 48us by R2-C4. If the monostable triggers on an equalising pulse, this monotime ensures that the next one is "skipped".

In principle, the monotime could be made a little shorter, but also a little longer, e.g. 62us or so, to eliminate the risk of IC2A being triggered by noise in the blanking period.

The three-digit binary line number supplied by the three counters is compared to the three-digit number set on the BCD switches. The line number word and switch word are applied in groups of 4-bits to the AN and BN inputs of three cascaded 4-bit comparators, type 74HCT85. The A=B output of the last comparator, IC8, goes high if the counted line number matches the number set on the BCD switches.

This instant marks the triggering of the oscilloscope timebase, so that the content of the relevant line is displayed. The actual trigger instant coincides with then end of the colour burst at about 4us after the positive edge of the line sync pulse.

The 5V regulated power supply of the circuit is standard and requires no further discussion. Provision is made to fit three different mains transformers, as will be discussed below.

# BACKGROUND TO VIDEO INSERTION TEST LINES (VIT)

VIT lines enable the quality of TV reception as well as the quality of TV and video equipment to be checked and optimised. A number of test signals are available, and their function is discussed briefly. The contents of the VIT lines are in accordance with the relevant recommendations for PAL G/B/I transmissions (CCIR Spec 624-2).

**Note:** the use and function of VIT lines are recommendations, not standards. Differences may therefore occur depending on the type of transmitter (terrestrial/satellite; high/low power; TV-band; etc.), as well as on services and broadcasting authorities.

**VIT lines 17 and 18 (Fig.1)**

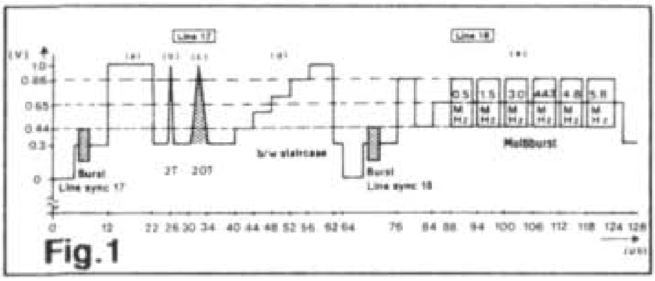


Fig.1

**(a)** *Reference bar* to establish maximum black and white levels. Test: LF-response of receive system.

**(b)** *2T-pulse* for picture resolution assessment. T is the shortest possible rise-time in a system in which the highest frequency of a sinusoidal signal is fc. Hence T = 1/2fc. In a PAL TV system fc = 5MHz so T = 0.1us. The 2T pulse has sinusoidal slopes and a width of 0.2us. Test: amplitude reduction of the 2T pulse with respect to the reference bar means loss of high frequencies in the system. For normal TV reception a loss of 20% is acceptable.

**(c)** *20T-pulse* for testing chrominance and luminance response and possible interactions between these components. The 20T pulse is actually a 20T long chrominance burst. Since 20T = 0.5MHz and the chrominance frequency is 4.43MHz, these components are affected differently by bandwidth limiting factors in the transmission system. Test: the 20T pulse serves to identify amplitude and phase distortion.

In Fig.2 the first response indicates chrominance amplitude reduced, the second different phase delays for chrominance and luminance, and the third response indicates a combination of both problems.

(d) *Monochrome Staircase* for linearity assessment. Steps are 140mV level increments. test: irregular step size means non-linearity.

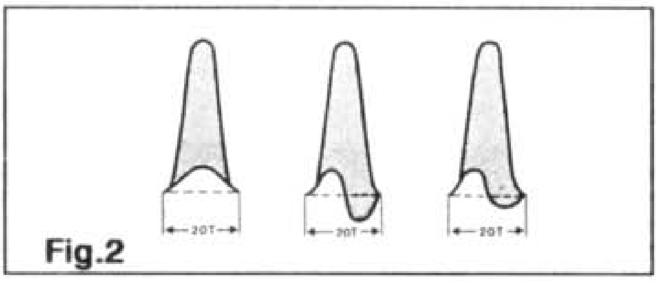


Fig.2

**(e)** *Multiburst* for frequency response measurement. The bursts have a nominal amplitude of 420mV p-p and are preceded by an 8us long 125kHz reference signal. Test: high-frequency loss is marked by reduced amplitude which is first noted with the last three bursts.

**VIT lines 330 and 331 (Fig.3)**

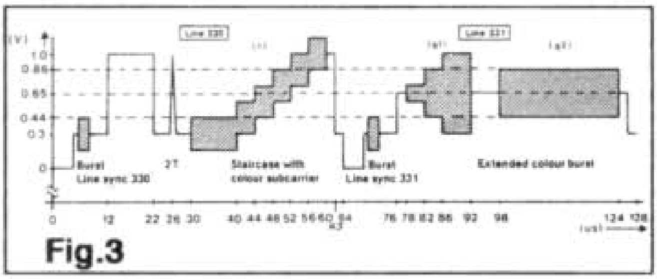
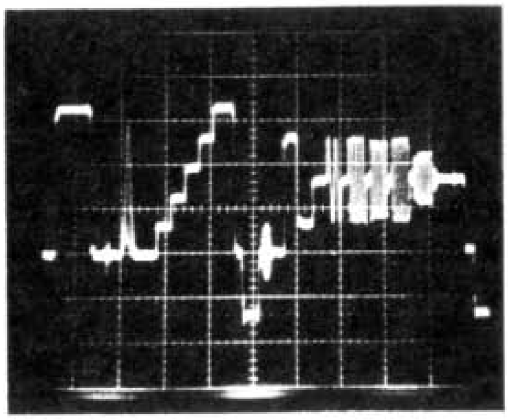


Fig.3

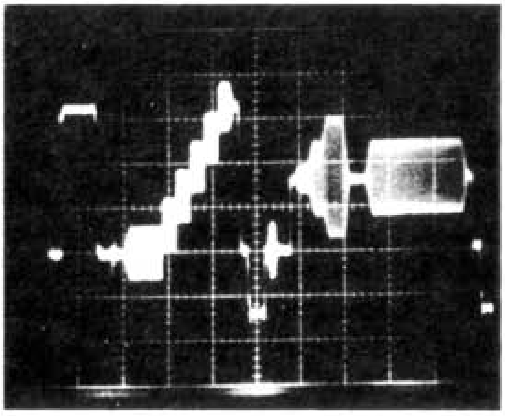
**(f)** *Staircase with Colour Subcarrier* for differential gain or phase error detection. The subcarrier level is 280mV p-p. Ideally, the colour separator in the receiver removes the luminance component and supplies a 30us long 4.43MHz burst of 280mV p-p. Test: phase or amplitude irregularities on the step instants (40-44-48-52-56us). Use an oscilloscope for amplitude test and a vectorscope for phase test.

**(g)** *Colour Subcarrier Signals and Extended Colour Burst* for measurement of intermodulation between chrominance and luminance components. After filtering out the chrominance subcarrier (4.43MHz), the luminance level should be constant at 0.65V. Test: amplitude irregularities occurring between 78-92us indicate intermodulation caused by chrominance changes (g1) or luminance changes (g2; subcarrier level of 420mV p-p).

Fig.4 shows the theory in practice. The upper oscillogram is of lines 17 and 18, and the lower oscillogram of lines 330 and 331. The oscilloscope used was an Iwatsu 100MHz model.



Lines 17 and 18



Lines 330 and 331

## CONSTRUCTION

The single-sided printed circuit board for this project is shown in Fig.5 (for details on obtaining the PCB see the end of this article). Depending on the enclosure you intend to use, it may have to be divided into two to separate the power supply section from the rest of the circuit.

Start the construction of the main board by fitting all 14 wire links, followed by the passive parts. The components in positions R4, R5 and R6 are preferably 4-resistor, 5-pin single-in-line (SIL) arrays. Discrete resistors may also be used if such arrays are difficult to obtain. In that case, fit four 47k resistors upright on the board and cut their free terminals short. Join the free terminals with a horizontally running wire that goes to the PCB hole marked with a dot.

Voltage regulator IC9 can make do without a heat-sink as it dissipates little heat.

IC sockets are not strictly required, but you may prefer to use them to make replacement of an IC easier if a fault is suspected.

Three different types of transformer may be fitted on the power supply board. The choice between these depends on availability and the mains voltage (U.K. 240V; other European countries 220V). For operation from 240V mains fit a 2 x 4.5V (1.2VA) transformer from RS Components. For 220V mains, use either a Block 1 x 9V (1.5VA) or a 2 x 6V (1.5VA) type. Install insulated wire links if necessary:

- RS 2 x 4.5V: B - F and A - C
- Block 1 x 9V: B - E and A - D
- Block 2 x 4.5V: A - C, B - F and D - E

The mains is connected to terminal block K1.

The choice of BCD switches is all yours. Thumbwheel switches with BCD outputs are available from several sources. Their only disadvantages are that they are usually relatively large and not as quick to operate as rotary types. Before connecting the BCD switches to the circuit, be sure that you know the pin assignment (A-B-C-D and +/common). A mistake here makes the selection of a particular video line a matter of chance. If in doubt, check out the pin functions of the switches you intend to use with a multimeter.

The inputs marked "1" on the PCB must be connected to the least-significant bit, i.e. the switch terminal whose output level changes every time the switch is operated. Similarly, the terminals that change every second, fourth and eighth switch turn are connected to the PCB pins marked 2, 4 and 8 respectively.

The PCB(s) and the BCD switches are fitted into a suitably sized ABS enclosure. The type shown in the photographs has outside dimensions of 165 x 115 x 75mm (L x W x H). A mains socket with integral fuse-holder is fitted on the rear panel.

Two video input sockets are fitted on the front panel to enable the line selector to be connected in parallel with an existing video link. Alternatively, a single BNC input socket may be fitted. In that case, a T-junction is used to make to make the parallel connection. The trigger output of the circuit is a BNC socket to allow ready use of the available test cables.

## PRACTICAL USE

Since the LM1881 has a maximum input voltage rating of 3V peak-to-peak, it is recommended to provide the input of the circuit with a 10klinear potentiometer as a level control. Remember that the input impedance of the LM1881 is about 10k, and the CVBS signal must be negative-going, i.e. the sync pulses point down and represent the lowest instantaneous voltage.

Connect the trigger output of the circuit to the external trigger input of the oscilloscope. The composite video signal is applied simultaneously to the line selector, the oscilloscope input and a video monitor, to assist in tuning to a TV station. Set the oscilloscope to external triggering, and select the TV H+ mode if available. Set the oscilloscope timebase to 20us. The oscilloscope should display three successive lines, starting with the number set on the line selector (line 17 is suitable for a start).

Finally, in view of the relatively fast signals that occur in TV pictures, particularly in the VIT lines, it is recommended that an oscilloscope is used which has a bandwidth of a least 20MHz. You will notice that a relatively high trace intensity setting is required for a close examination of the test line contents.

A printed circuit board for this project is available from Elektor Electronics (Publishing), Down House, Broomhill Road, London, SW18 4JQ. The reference number is: 900032 and the price including VAT and p&p is £8.48.

### COMPONENTS LIST

| | | |
|---|---|---|
| **Resistors:** | | |
| 1 | 680k | $R_1$ |
| 1 | 68k | $R_2$ |
| 1 | 27k | $R_3$ |
| 3 | 47k 4-way SIL array | $R_4$;$R_5$;$R_6$ |
| **Capacitors:** | | |
| 9 | 100n | $C_1$;$C_2$;$C_8$–$C_{14}$ |
| 1 | 100n ceramic | $C_3$ |
| 2 | 1n0 | $C_4$;$C_5$ |
| 1 | 100µ 25V radial | $C_6$ |
| 1 | 10µ 10V radial | $C_7$ |
| **Semiconductors:** | | |
| 4 | 1N4001 | $D_1$;$D_2$;$D_3$;$D_4$ |
| 1 | LM1881 | $IC_1$ |
| 1 | 74HCT221 | $IC_2$ |
| 3 | 74HCT162 | $IC_3$;$IC_4$;$IC_5$ |
| 3 | 74HCT85 | $IC_6$;$IC_7$;$IC_8$ |
| 1 | 7805 | $IC_9$ |
| **Miscellaneous:** | | |
| 1 | mains transformer. Options: VR1109 (Block) or 207-863 (RS components (see text). | |
| 1 | PCB terminal block | $K_1$ |
| 1 | BNC or phono socket | $K_2$ |
| 1 | BNC socket | $K_3$ |
| 1 | PCB | 900032 |